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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
LE, THONG QUOC

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

[redacted]

Office Acti n Summary	Application No. 09/823,642	Applicant(s) MAK ET AL.	
	Examiner Thong Q. Le	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 14-17* is/are rejected.

7)☒ Claim(s) *9-13 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

[redacted]

DETAILED ACTION

Claims 1-18 are presented for examination.

Specification

1. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "**multiplexer in claim 18**" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1,6,8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 1, 6 and 8 recites the limitation "the voltage level" in claim 1,6, 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claim 17** is rejected under 35 U.S.C. 102(b) as being anticipated by Saito (U.S. Patent No. 5,708,598).

In regard to claim 17, Saito discloses a comparator circuit (Figure 1, 104 A) in a memory array (Figure 1) comprising:

a first input coupled to a first bit line that is coupled to a first memory cell in the memory array (Figure 1, Figure 2 show first input of comparator 104A coupled to first bit line 116A of first memory cell 202 in the memory array 201 in Figure 2) ;

a second input coupled to a second bit line that is coupled to a second memory cell in the memory array (Figure 1, Figure 2 show second input of comparator 104A coupled to second bit line 118A, and coupled to second memory cell 202 in memory array 201); and

an output coupled to a sticky latch (Figure 1, output 132 A of comparator 104A coupled to sticky latch 130).

[redacted]

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 1- 8, 14-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito (U.S. Patent No. 5,708,598) in view of Stave et al. (U.S. Patent No. 6,002,623).

In regard to claims 1-2, Saito discloses an apparatus, comprising:

a first memory cell (Figure 2, 202 in 201_0) coupled to a first bit line (Figure 2, 116B);

a second memory cell (Figure 2, 202 in 201) coupled to a second bit line (Figure 2, 118B); and

a comparator circuit (Figure 2, 104B) coupled to the first and second bit lines (Figure 1, 116A, 118A, Column 3, 35-38) to compare the voltage level on the first bit line with the voltage level on the second bit at a time when data is output from the first memory cell on the first bit line and from the second memory cell on the second bit line (Column 6, lines 37-49, Column 7, lines 8-12).

Saito as described above, fails to disclose an address decoder coupled to the first and second memory cells to enable access to the first and second memory cells. However, Stave et al. discloses an address decoder (Figure 2, 130) coupled to the first and second memory cells (Figure 1, MC, *first memory cells coupled to first bit line 105*,

second memory cells coupled to second bit line 106) to enable access to the first and second memory cells (Column 2, lines 59-61, Column 4, lines 2-4).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to make an address decoder coupled to the first and second memory cells to enable access to the first and second memory cells, since address decoder must have in a memory device, address decoder is used to provide a select signal to determine a memory address in a memory cell array for reading a data from or writing a data to cell of memory array. Address decoder is seen to be inherent in a memory device.

Therefore, it would have been obvious to combine Saito with Stave et al. to obtain the invention as specified in claim 1.

In regard to claim 3, Saito discloses wherein the first and second memory cells are dynamic RAM memory cells (Column 1, 27).

In regard to claim 4, Saito fails to disclose wherein the first and second memory cells are static RAM memory cells. However, Stave et al. disclose the first and second memory cells are SRAM (Column 1, lines 22-24).

At the time the invention was made, it would have been an obvious to a person of ordinary skill in the art to use SRAM cells in a memory device. Applicant has not disclosed that SRAM cells in memory device provides an advantage, is used for a particular purpose, or solves a stated problem. It would have been an obvious design choice to use SRAM cells in memory device, since SRAM cells are manufactured with a storage capacity is less than storage capacity of DRAM and needing more power than

DRAM, furthermore, when the SRAM cells substituted DRAM cells, the remaining elements still perform the same function as DRAM cells are used.

Therefore, it would have been obvious to a person of ordinary skill in this art to combine Saito with Stave et al. to obtain the invention as specified claim 4.

In regard to claim 5, Saito discloses wherein the comparator circuit is comprised of a single comparator (Figure 1, 104A) with a first input coupled to the first bit line (Figure 1, 116A) and a second input coupled to the second bit line (Figure 118A, Column 6, lines 41-45) (*Figure 1, shows two bit lines 116A and 118A coupled to two inputs of comparator 104A*) .

In regards to claim 6, Saito discloses wherein the output of the comparator (Figure 1, 132A) is coupled to a latch (Figure 1, 130) to store an indication that the voltage level on the first bit line differs substantially from the voltage level on the second bit line (Column 7, lines 8-17, *output signal from comparator by comparison between two bit lines then send output signal to latch 130 and latch 130 determine the value of bit lines*).

In regard to claim 7, Saito discloses wherein the time at which the latch is triggered is adjustable (Column 7, lines 14-24, *the latch is adjusted until determining the bit values represented by a voltage in a memory cell*)

In regard to claim 8, Saito discloses wherein the latch is a sticky latch that is triggered to latch an indication that the voltage level on the first bit line differs substantially from the voltage level on the second bit line at any time that such an indication takes place (Column 7, lines 45-65, Column 8, lines 19-24, *latch (controller)*

latch an indication after comparing voltage level of first bit line (primary bit line 116 in Figure 1) with voltage level of second bit line (complementary bit line 118 in Figure 1)) .

In regard to claims 14-15, the apparatus discussed in claims 1, 5 and 6 above would perform the claims 14-15.

In regard to claim 16, Saito disclose setting the degree to which the difference in voltage levels between the first bit line and the second bit line is substantial (Column 8, lines 21-23, Column 8, lines 56-65, Column 13, lines 35-36, Column 9, lines 47-50).

Allowable Subject Matter

10. **Claims 9-13, 18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9-13 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Saito (U.S. Patent No. 5,708,598), Stave et al. (U.S. Patent No. 6,002,623), and others, does not teach the claimed invention having comparator in Figure 2 including a subtracting circuit 390 with a first input coupled to the first bit line 370 and second input coupled to a second bit line 372 , and a first comparator 340 and second comparator 341 coupled to output from subtracting circuit 390.

Claim 18 includes allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Saito (U.S. Patent No. 5,708,598), Stave et al. (U.S. Patent No. 6,002,623),

and others, does not teach the claimed invention having a multiplexer to disconnected the second bit line (Figure 2, 276) and connected to a third bit line (Figure 2, 270) that is coupled to the first memory cell (Figure 2, 260) in the memory array (Figure 2, 210).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 703-306-9123. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Thong Q. Le
Examiner
Art Unit 2818

April 4, 2002